Design of an MPEG-based set-top box for video on demand services

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Abstract:

Presents the design of an MPEG-based set-top box for digital video decoding and interfacing with the ADSL-based network or fiber-coaxial network. The architecture of the set-top box consists of three major functional blocks: the central control unit, the digital video decoding unit and the network interface unit. A universal bus is used to connect these blocks and other add-on peripheral modules. Based on this bus, an extension slot is implemented to enhance the design flexibility in supplementing functionality and upgrading performance, such as the improvement from the original 1.544 Mbps T1 interface to a higher throughput network interface in order to provide high quality MPEG 2 video on demand (VOD) services.

Subject Terms:

interactive television; interactive systems; cable television; optical fibre subscriber loops; digital television; optical communication equipment; telecommunication terminals; telecommunication services; decoding; video signal processing; video equipment; telecommunication control; channel capacity; MPEG-based set-top box; video on demand services; design; digital video decoding; ADSL-based network; fiber-coaxial network; central control unit; network interface unit; universal bus; add-on peripheral modules; extension slot; performance; throughput; high quality MPEG 2; 1.544 Mbit/s

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DESIGN OF AN MPEG-BASED SET-TOP BOX FOR VIDEO ON DEMAND SERVICES

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ABSTRACT

In this paper, we present the design of an MPEG-based set-top box for digital video decoding and interfacing with the ADSL-based network or fiber-coaxial network. The architecture of the set-top box consists of three major functional blocks: the central control unit, the digital video decoding unit and the network interface unit. A universal bus is used to connect these blocks and other add-on peripheral modules. Based on this bus, an extension slot is implemented to enhance the design flexibility in supplementing functionality and upgrading performance, such as the improvement from the original 1.544 Mbps T1 interface to a higher throughput network interface in order to provide high quality MPEG II video on demand (VOD) services.

1. INTRODUCTION

The set-top box serves as an important application of the MPEG[1] video decoder due to its potentially wide-spread use at every residential household in the forthcoming VOD service[2][3][4]. Fig. 1 shows a typical application of this set-top box in the ADSL-based[5] telephone network. Since video services are projected to carry the majority of the overall traffic on the information highway, the design of a set-top box is essential to the development of the National Information Infrastructure. Therefore, The design goals of a set-top box architecture[6] should include the following:

- Long-term utilization: The set-top box must be operational over a life span of at least 8 years.
- Cost-effectiveness: Any standard must support a solution of low cost and minimal feature set.
- Expandability: Manufacturers should support the optional value-added features that can be provided without violating the standard.
- Compatibility: The set-top box may provide as many access modes as possible, such as twisted pairs (T1, ADSL) , coaxial cable, wireless, etc., in order to be compatible in various service platforms.
- Data independency: In addition to the data types known today, new service types must be considered in the future as an integrated part in our design.

According to the above considerations, we design the set-top box with the following special features. A universal bus is used to interconnect the functional modules to enhance the system flexibility. An extension slot consists of address, data, interrupt and DMA signals is implemented and memory space is reserved to easily accommodate any kinds of add-on peripheral modules, such as the fiber-coaxial network interface, cable modem interface and other value-added functional modules. A T1 module, which is connected with the main circuit board via a 50-pin connector, is implemented as the default network interface in order to provide the 1.5Mbps bandwidth for transmissions of MPEG I digital video programs over the T1 or ADSL network. The MPEG decoder adopted in this design is a single-chip programmable processor[7] capable of supporting the MPEG I or MPEG II video decompression standard. This decoder chip is able to sustain higher bit rate (3~6 Mbps) decoding in the future. A low cost 32-bit integrated processor[8] with built-in timers, serial ports and DMA's is adopt as the central control unit in order to reduce the additional cost of off-chip timer IC, serious modules, etc.

The software aspect of our set-top box features a layered architecture. It is easy to modify this software while additional hardware modules or software protocols are appended.

2. HARDWARE ARCHITECTURE OF THE SET-TOP BOX

The primary function of the set-top box is to provide a gateway to the interactive service and also provide a user friendly interface for controlled access. The architecture shown in Fig. 2 meets the above requirements and is the functional architecture of our set-top box. Some essential functional blocks are explained in the following sections.

2.1 Integrated CPU MC68340

This is the control unit of the set-top box and runs at the speed of 25MHz. It is primarily implemented by using an integrated microprocessor MC68340. It executes software programs to manage the overall system and deal

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with the reception, buffering and display of data. The serial port offered by the processor is used to connect the service provider via the control signal line. This serial connection is a bi-directional RS-232 interface with a maximum bit rate of 19.2 kbps.

2.2 Universal Bus

The universal bus contains all of the necessary bus signals of the system, including address, data, and control lines. It is clearly defined to easily accommodate additional add-on peripheral modules.

2.3 Extension Slot

The extension slot is a 62-pin bus slot implemented on the main circuit board. It contains 4096 decoded addresses (12 address lines), 16-bit wide data lines, 3 interrupt request lines, 2 DMA channels and other bus control signals. There is enough space reserved in the set-top box to allow the allocation of extra extension cards on the main circuit board via the extension slot.

2.4 pLSI 1032 Module

The pLSI 1032 module contains a complex PLD pLSI 1032[9] and its corresponding bus buffer. The pLSI 1032 with the density of 6000 gates is programmed to be the address decoder and control gates of the MC68340.

2.5 Remote Control Module

This module is used to receive and decode the control signals or the user's commands coming from the infra-red remote controller or the buttons on the front panel. It is implemented with a low cost single-chip microcomputer module, efficient in decoding infra-red signals. The remote control module can be programmed to accept additional types of control when more function keys are required in the future. Basically, we provide the ordinary VCR function keys and some special keys for the purpose of interactive service, such as 'demand program', 'menu page up', 'menu page down' on the remote controller and the front panel of the set-top box.

2.6 LCD Display

The functional block is used to display the operational information related to the set-top box. However, all of the information, including text, graphics and video can be displayed on the TV set through the MPEG decoder module. The LCD panel is used to display simple messages.

2.7 T1 Module

The T1 module is implemented on a daughter board which connects the main circuit board via a connector. Fig. 3 shows the detailed architecture of this module. The LIU[10] block and T1 framer[11] block form the physical layer. The HDLC controller[12] block forms the data link layer. With the T1 control logic block, the control unit can access the internal registers of the LIU and T1 framer. The unidirectional video bit stream data which comes from the service provider is stored in the external shared memory block. The control unit access this memory to get the bit stream for further processing. When an error occurs during the reception of the video bit streams, the corresponding error status is stored in the status FIFO and an interrupt request is issued to the control unit that monitors the T1 module.

2.8 RAM EPROM Area

This block presents the main memory area of the control unit. It is used to store the software programs and buffer the bit stream data.

2.9 MPEG Decoder

The MPEG decoder block is implemented with a powerful MPEG processor. Fig. 4 shows the detailed functional architecture of the MPEG decoder. The MPEG playback processor is a software programmable chip used to decode the video and audio data from the MPEG system stream. It supports graphic overlay of text or bit maps. Therefore, the demand information, such as menu screen, system message can be shown on the TV screen. The processor uses two kinds of external memory. One is the SRAM block and the other is the DRAM block. The SRAM block is used to store the microcoded program and also serve as cache buffers. The DRAM block is used to stored the bit stream data and the decoded image frames. The decoded image frame will be sent to the video encoder for generating the standard NTSC/PAL video signals. The decoded audio signals are sent to the PCM DAC block to be converted to analog signals. Finally, the audio analog signal is amplified by the op amp block.

3. SOFTWARE ARCHITECTURE OF THE SET-TOP BOX

In the set-top box, there are three portions needed to be programmed: the integrated CPU MC68340 module, the remote control module and the MPEG decoder module. The software code of the MPEG decoder is basically programmed to decode the MPEG I data stream

with the development kit provided by the chip provider. This software code called VC code is stored in the EPROM and is downloaded to the module while the set-top box is initialized. The program of the remote control module is stored on the EPROM memory of the module. It is programmed to scan the keys on the front panel and decode the infra-red signals from the remote controller. The decoded message or command is sent to the control unit with an interrupt request to the integrated CPU MC68340. The integrated CPU MC68340 module forms the control unit of the set-top box. Its software architecture is described as follows.

3.1 Software architecture of the control unit

The software in the control unit for communications and routing is used to provide an intelligent interface between the peripherals and the service provider. Fig. 5 shows the software architecture of the control unit. The lowest layer is the physical layer driver for each hardware module. The communication protocol management program deals with the communication issue . The buffer management program deals with incoming bit stream data and buffer control. The command interpreter bridges over the above mentioned programs and the upper application layer program, interpreting the commands in the application program or commands coming from the remote control module. The application program contains all the necessary commands to control the set-top box.

4. EXPERIMENTAL RESULTS

The VOD prototype system[13][14] built at Telecom Lab shows that a set-top box must perform the function of traffic smoothing while converting data between the service provider and the user. It acts as a communication interface to the service provider, a router for controlling data flow and an intelligent device for the compatibility mechanism between data types and system capacities. Therefore, we set up the same T1 module and MPEG decoder on the PC computer to simulate the functions of the set-top box. The system bit stream is provided from a video server connected to the PC via a T1 line. The experimental results show that the set-top box provides a convenient, real-time interactive user interface while sustaining smooth video display quality without visible delay or jitters by adequately applying buffering techniques.

5. CONCLUSIONS

In this paper, we have shown the architecture of an MPEG-based set-top box which conforms to the design goals. The prototyping set-top box is under extensive development and performance enhancement. The software subroutines are first tested in the PC environment and then exported to the set-top box. This set-top box will be used in the VOD field trial by our laboratory to examine its interoperability with the ADSL-based telephone network.

6. ACKNOWLEDGMENT

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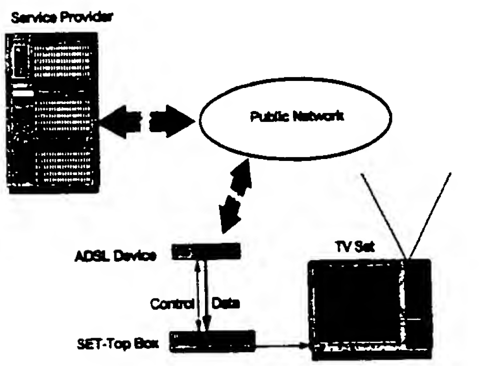

Fig. 1 A typical application of the set-top box

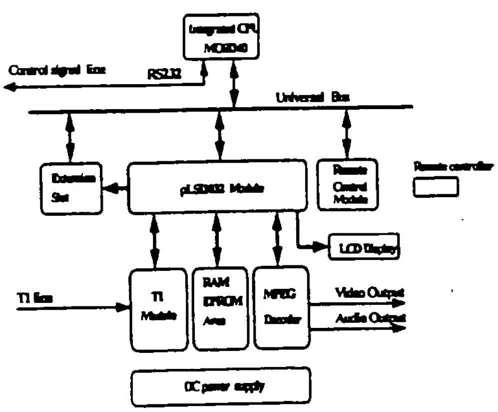

Fig. 2 Functional architecture of the set-top box

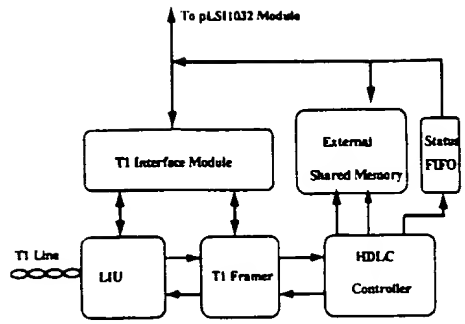

Fig. 3 Functional architecture of the T1 module

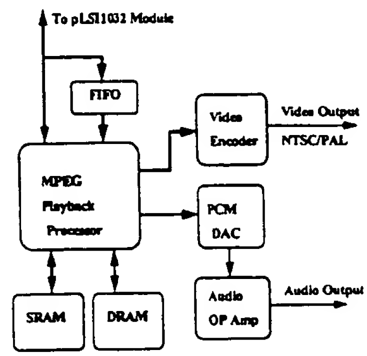

Fig. 4 Functional architecture of the MPEG decoder

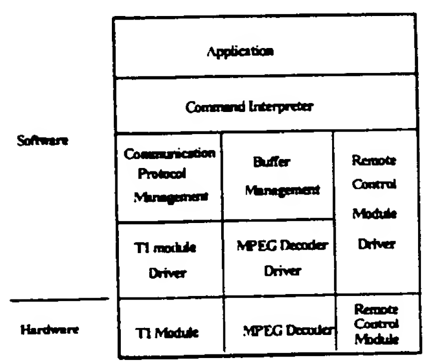

Fig. 5 Software architecture of the control unit